CLAIMS

1. A method for testing a circuit, said method comprising:

serially shifting a test pattern into at least a portion of the circuit;

disabling each of a plurality of tristate drivers except a default driver from the plurality of tristate drivers while serially shifting;

capturing a test response from at least a portion of the circuit; and

disabling each of the plurality of tristate drivers except a selected one of the plurality of drivers while capturing the test response.

2. The method of claim 1, further comprising:

receiving a selection indicating the selected one of the plurality of drivers.

3. The method of claim 2, wherein the selection is a function of the test pattern.

4. The method of claim 1, wherein disabling each of the plurality of tristate drivers except the default driver further comprises transmitting a signal with a first logic state to logic controlling the default driver and transmitting a signal with a second logic state to logic controlling each of the plurality of tristate drivers except the default driver.

5. The method of claim 4, wherein the logic controlling each of the tristate drivers receives functional enable signals.

6. The method of claim 4, wherein the circuit has a testing mode of operation and a functional mode of operation, the method further comprising:

transmitting a signal with the first logic state to logic controlling each of the plurality of tristate drivers during the functional mode.

7. The method of claim 6, wherein the functional mode is indicated by receiving a deasserted signal.

8. A system for testing a circuit, said system comprising:

scan line registers for shifting a test pattern into at least a portion of the circuit and capturing a test response from at least a portion of the circuit;

a decoder for disabling each of a plurality of tristate drivers except a default driver from the plurality of tristate drivers while the scan line registers serially shift the test pattern, and disabling each of the plurality of tristate drivers except a selected one of the plurality of drivers while the scan line registers capture the test response.

9. The system of claim 8, wherein the scan line registers provide a selection indicating the selected one of the plurality of drivers to the decoder.

10. The system of claim 9, wherein the selection is a function of the test pattern.

11. The system of claim 8, further comprising:

a plurality of logic circuits, each of the plurality of logic circuits for controlling an associated one of the plurality tristate drivers, the logic circuits disabling the associated one of the plurality of tristate drivers when receiving a signal with a first logic state.

12. The system of claim 11, wherein the logic circuits comprise an input for receiving a functional enable signal.

13. The system of claim 11, wherein the circuit has a testing mode of operation and functional mode of operation, the decoder transmitting a signal with the second logic state to each of the plurality of logic circuits controlling each of the plurality of tristate drivers during the functional mode.

14. The system of claim 13, wherein the decoder comprises an input for receiving a signal indicating the functional mode or the testing mode.

15. A circuit for testing a device under test, said circuit comprising:

scan line registers shifting a test pattern into at least a portion of the device under test and capturing a test response from at least a portion of the circuit;

a decoder connected to the scan line registers, the decoder disabling each of a plurality of tristate

drivers except a default driver from the plurality of tristate drivers while the scan line registers serially shift the test pattern, and disabling each of the plurality of tristate drivers except a selected one of the plurality of drivers while the scan line registers capture the test response.

16. The circuit of claim 15, wherein the scan line registers provide a selection indicating the selected one of the plurality of drivers to the decoder.

17. The circuit of claim 16, wherein the selection is a function of the test pattern.

18. The circuit of claim 15, further comprising:

a plurality of logic circuits, each of the plurality of logic circuits connected to an associated one of the plurality tristate drivers, the logic circuits disabling the associated one of the plurality of tristate drivers when receiving a signal with a first logic state.

19. The circuit of claim 18, wherein the logic circuits further comprise an AND gate.

20. The circuit of claim 18, wherein the logic circuits comprise an input receiving a functional enable signal.

21. The circuit of claim 18, wherein the device under test has a testing mode of operation and functional mode of operation, and the decoder transmits a signal with a second logic state to each of the plurality of logic circuits

controlling each of the plurality of tristate drivers during the functional mode.

22. The circuit of claim 21, wherein the decoder comprises an input receiving a signal indicating the functional mode or the testing mode.